Remarks:

Applicants (hereinafter, Applicant) hereby request reconsideration of the application.

Claims 1-28 remain in the application. Claims 25-28 have been added. No new matter is added. Claim 24 is withdrawn from consideration.

Amended claim 1 includes connection pieces, which cover the contact holes through the blocker layer. Additionally, claim 1 contains further contact holes filled with metal, which are arranged in the isolation layer. The further contact holes 330, 340 connect to at least one of the connection leads, and also connect to the connection pieces 250, 260. See Fig. 1.

Regarding claims 25-26, the contact holes can be made of tungsten or copper. For support, see page 18, lines 4-5 of the specification of the instant application.

Regarding claim 27, see Fig. 2, wherein the connection piece 310 is arranged above the blocker layer 160.

Regarding claim 28, see Fig. 4, wherein the connection piece 750 is arranged below the blocker layer 660.

In item 4 on page 2 of the above-identified Office action, the title has been objected to as being nondescriptive. In response, the title has been changed to --INTEGRATED CIRCUIT HAVING A DIFFUSION BLOCKER CONFIGURED AS A BLOCKER LAYER AND CONNECTION PIECES COMPOSED OF ALUMINUM COVERING CONTACT HOLES AND METHODS FOR FABRICATING THE SAME--.

In item 5 on page 2 of the Office action, claims 1-7 & 18 have been rejected as being fully anticipated by Bothra et al. (U.S. Pat. No. 5,798,559) (hereinafter, "Bothra") under 35 U.S.C. § 102.

In item 6 on page 4 of the Office action, claims 1-7 & 14-23 have been rejected as being obvious over Chiang et al. (U.S. Pat. No. 5,739,579) (hereinafter, "Chiang") in view of Oda (U.S. Pat. No. 6,060,784), Hayashide (U.S.Pat.No.5,500,558) and Tottori (U.S. Pat. No. 5,479,054) under 35 U.S.C. § 103.

As will be explained below, it is believed that the claims were patentable over this cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia, an integrated electrical circuit, comprising:

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impedes and prevents a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in at least one of a region having contact holes formed therein and a region of said connection pieces, said blocker layer disposed between said at least one element structure plane and said insulation layer;

said connection pieces being made of aluminum and covering said contact holes;

said connection pieces being covered by said isolation layer; and

a plurality of further contact holes being formed in said isolation layer and being filled with a metal, said metal being connected to at least one of said connecting leads. (Emphasis added.)

Accordingly, in the *present invention*, at least one diffusion blocker is disposed underneath the connecting leads; the diffusion blocker impedes the diffusion of copper. The integrated electrical circuit is configured such that the diffusion blocker is configured as a blocker layer, which is interrupted only in the region of contact holes or *connection pieces* and that the blocker layer is situated between the element structure plane and the insulation layer.

Further, the *present invention* teaches connection pieces, which cover the contact holes through the blocker layer. Additionally it includes further contact holes, filled with metal, which are arranged in the isolation layer. The further contact holes 330, 340 connect to at least one of the connection leads, and also connect to the connection pieces 250, 260, as recited in claim 1 of the instant application. See also Fig. 1.

In the *Oda* reference, an interconnection layer extends across a macro cell region and a circuit region other than the macro cell region. The macro cell region and the circuit region are monolithically integrated into a semiconductor device, *wherein the interconnection layer in the macro cell region is thinner than the interconnection layer in the circuit region.*

The *Hayashide* reference discloses *reducing a difference in level in a short time at a convex pattern, spreading horizontally on a large scale, and obtaining a semiconductor device having a planarized surface.* An insulating film is formed on a semiconductor substrate to cover a horizontally spreading convex pattern and to fill in a concave portion.

There, a portion of insulating film located on a planarized portion of convex pattern is selectively etched away so as to leave a frame-shaped insulating film having a certain width on the outer periphery portion of convex pattern. The insulating film, which is left on the semiconductor substrate is etched by a chemical polishing method, thereby planarizing a surface of the semiconductor substrate.

In the *Tottori* reference, a polycrystalline silicon film is formed on the surface of a semiconductor substrate. An oxide film having a first impurity concentration is formed to cover the polycrystalline silicon film. A polycrystalline silicon film and a refractory metal silicide are formed on the surface of the oxide film having the first impurity concentration. An oxide film having a second impurity concentration higher than the first impurity concentration is formed to cover the polycrystalline silicon film and the refractory metal silicide. *The third conductive layer is formed on the surface of the oxide film having the second impurity concentration.*

The *Bothra* reference discloses a method of making an integrated circuit interconnect structure having air as the effective dielectric between metallization layers including the steps of: a) providing an air dielectric formation layer of a sacrificial material over a substrate; b) forming a pillar holes in the air dielectric formation layer; c) filling the pillar holes with a non-sacrificial material; d) constructing a metallization layer over the sacrificial air dielectric formation layer and nonsacrificial material pillars; and e) applying an isotropic etchant to the interconnect structure to remove the sacrificial material, leaving the non-sacrificial material pillars for mechanical support of the metallization layer. *An interconnect structure having an air dielectric includes a bottom metallization layer, a top metallization layer, and a plurality of pillars separating the bottom and top metallization layers and mechanically supporting the top metallization layer.*

In other words, in the *Bothra* reference, *there is no connection piece, which is made of aluminum, in contrast to claim 1 of the instant application.* For example, the metallization layer 118 is formed in a three-stop process in order to form a TiN- Al/Cu-TiN structure. See col. 5, lines 60++. In the *Chiang* reference, there is no connection piece at all. On the contrary, the copper layer 120 is directly

connected to the tungsten plaque 41, in contrast to claim 1 of the instant application. See Fig. 12, Chiang.

Clearly, the references do not show "*said diffusion blocker configured as a blocker layer interrupted only in at least one of a region having contact holes formed therein and a region of said connection pieces, said blocker layer disposed between said at least one element structure plane and said insulation layer; said connection pieces being made of aluminum and covering said contact holes; said connection pieces being covered by said isolation layer; and a plurality of further contact holes being formed in said isolation layer and being filled with a metal, said metal being connected to at least one of said connecting leads*", as recited in claim 1 of the instant application (emphasis added). Thus, neither can the specific combination of the aforementioned limitations be shown.

In other words, the features including the limitations "*said diffusion blocker configured as a blocker layer interrupted only in at least one of a region having contact holes formed therein and a region of said connection pieces, said blocker layer disposed between said at least one element structure plane and said insulation layer*", "*said connection pieces being made of aluminum and covering said contact holes*", "*said connection pieces being covered by said isolation*

layer", and "a plurality of further contact holes being formed in said isolation layer and being filled with a metal, said metal being connected to at least one of said connecting leads", as recited in claim 1, attain the present invention's objectives and are not taught or suggested by the references, whether taken alone or in any combination (emphasis added).]

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

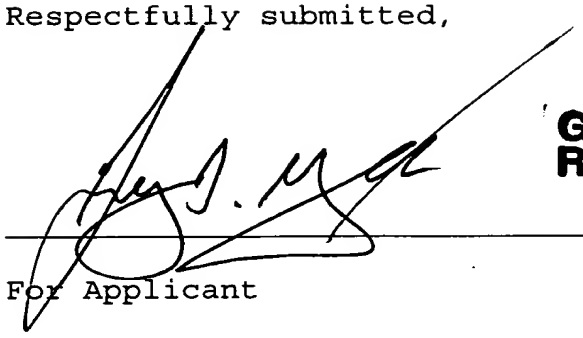
In view of the foregoing, reconsideration and allowance of claims 1-28 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

Please change the title "Integrated Electrical Circuit and Method for Fabricating It" to --INTEGRATED CIRCUIT HAVING A DIFFUSION BLOCKER CONFIGURED AS A BLOCKER LAYER AND CONNECTION PIECES COMPOSED OF ALUMINUM COVERING CONTACT HOLES AND METHODS FOR FABRICATING THE SAME--.

In the claims:

Claim 1 (amended). An integrated electrical circuit, comprising:

a plurality of structure planes including at least one element structure plane;

electrically active elements disposed on said at least one element structure plane;

at least one insulation layer disposed above said at least one element structure plane;

electrical connecting leads disposed at least one of within and above said insulation layer, at least a portion of said electrical connecting leads contain copper;

connection pieces disposed underneath said electrical connecting leads; [and]

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impedes and prevents a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in at least one of a region having contact holes formed therein and a region of said connection pieces, said blocker layer disposed between said at least one element structure plane and said insulation layer[.];

said connection pieces being made of aluminum and covering said contact holes;

said connection pieces being covered by said isolation layer; and

a plurality of further contact holes being formed in said isolation layer and being filled with a metal, said metal being connected to at least one of said connecting leads.